

ABSTRACT OF THE DISCLOSURE

An operational amplifier has a differential amplifier stage comprising a pair of first PMOS transistors for inputting signals, which are arranged between a positive voltage supply coupled with a first constant current source and a negative voltage supply, wherein second PMOS transistors of a high voltage resistant type, gates of which are biased to a prescribed voltage, are arranged on current paths lying between the first PMOS transistors and the negative voltage supply together with load resistors. Herein, each of drain voltages of the first PMOS transistors is limited to a certain value that is higher than the prescribed voltage by a gate threshold voltage. Therefore, even when the first PMOS transistors are configured of a normal voltage resistant type, it is possible to reliably prevent voltages applied to the first PMOS transistors from exceeding breakdown voltages thereof, thus avoiding unnecessary reduction of an S/N ratio.